In this assignment, you will use the Altera tools to develop synchronous designs, as well as take advantage of hierarchy (using library functions).

1. Tutorial II: Sequential Design and Hierarchy. Install the UP1core and tutorial files from your CD onto your network drive. Before downloading the design, simulate it (at the end of section 4.4). Finish the tutorial, and demonstrate that it works on the UP 1 board. For this part, you should turn in the simulation of the original circuit, and a printout of the revised circuit with a signature from me that I saw it work correctly.

2. Exercise 4 on page 61 (a hex stopwatch). Turn in: a document that describes your design and any design decisions, a (reasonable-sized) printout of the schematic (signed by one of the TA’s or me to show that you downloaded the design and it works), an annotated printout of the simulation output that shows that the circuit works as expected, and a printout of any appropriate timing analysis. Again, the circuit that you simulate will not be quite the same as the circuit that you download (e.g. only the downloaded circuit will contain the debouncer).

3. Exercise 6 on page 62. Use the "74160" function from the library for your BCD counter. Again, turn in the signed schematic, simulation output and timing analysis, as well as a document that describes your design and any design decisions that you made.